

1 1. A method for routing a data frame through a
 2 fibre channel fabric, said fibre channel fabric
 3 comprising a switch having a plurality of ports, said
 4 ports are operative for transmitting and receiving
 5 said data frame, said method comprising:
 6 receiving said data frame at a first port of said
 7 switch;
 8 writing said data frame to a shared memory location,
 9 said shared memory location is coupled to at least two of
 10 said plurality of ports of said fibre channel switch;
 11 identifying a second port of said switch, said
 12 second port operative for transmitting said data frame
 13 from said shared memory location;
 14 transmitting a message from said first port to said
 15 second port indicating the position in said shared memory
 16 location of said data frame; and
 17 at said second port, reading said data frame from
 18 said memory, wherein said switch has more than one rate
 19 for reading and writing data.

1 2. The method of claim 1, wherein said shared
 2 memory location is implemented using a plurality of SRAM
 3 modules, one or more SRAM module for each of said
 4 plurality of fibre channel ports.

1 3. The method of claim 2, wherein said plurality
 2 of fibre channel ports is an odd number of fibre channel
 3 ports.

1 4. The method of claim 1, wherein said shared
 2 memory comprises a plurality of columns and wherein each
 3 of said plurality of fibre channel ports has access to
 4 one of said plurality of columns.

1 5. The method of claim 4, wherein said access
 2 occurs during a clock cycle.

1 6. The method of claim 4, wherein said access
2 occurs during a 106.25 MHz clock cycle.

1 7. The method of claim 4, wherein said plurality
2 of columns comprises a plurality of SRAM modules.

1 8. The method of claim 4, wherein said plurality
2 of fibre channel ports have a read access during a first
3 clock cycle and a write access during a second clock
4 cycle, said second clock cycle immediately follows said
5 first clock cycle.

1 9. The method of claim 1, wherein said shared
2 memory location supports both a 1 gigabit per second and
3 a 2 gigabit per second read and write data rate.

1 10. A method for providing a shared memory location
2 in a fibre channel fabric, said fibre channel fabric
3 comprising a fibre channel switch having a plurality of
4 fibre channel ports, said fibre channel ports are
5 operative for transmitting and receiving said data frame,
6 said method comprising:

7 receiving said data frame at a first fibre channel
8 port of said fibre channel switch;

9 writing said data frame in said shared memory
10 location, said shared memory location coupled to each of
11 said plurality of fibre channel ports; and

12 reading said frame from said shared memory location
13 into a second fibre channel port, wherein said fibre
14 channel switch has more than one rate for reading and
15 writing data.

16 and, transmitting said data frame the second fibre
17 channel port, wherein said writing and reading are
18 performed in a manner that is dependent on the relative
19 rates at which said frame is received and transmitted.

1 11. The method of claim 10, wherein said shared
2 memory location is implemented using a plurality of SRAM
3 modules, one or more SRAM module for each of said
4 plurality of fibre channel ports.

1 12. The method of claim 11, wherein said plurality
2 of fibre channel ports comprises an odd number of fibre
3 channel ports.

1 13. The method of claim 10, wherein said shared
2 memory location comprises a plurality of columns and
3 wherein each of said plurality of fibre channel ports has
4 access to one of said plurality of columns.

1 14. The method of claim 13, wherein said access
2 occurs during a clock cycle.

1 15. The method of claim 13, wherein said access
2 occurs during a 106.25 MHz clock cycle.

1 16. The method of claim 13, wherein said plurality
2 of columns comprises a plurality of SRAM modules.

1 17. The method of claim 13, wherein said plurality
2 of fibre channel ports have a read access during a first
3 clock cycle and a write access during a second clock
4 cycle, said second clock cycle immediately follows said
5 first clock cycle.

1 18. The method of claim 10, wherein said shared
2 memory location supports both a 1 gigabit per second read
3 and write data rate and a 2 gigabit per second read and
4 write data rate.

1 19. A fibre channel fabric comprising:
2 a fibre channel switch having a plurality of fibre
3 channel ports embodied thereon for transmitting and
4 receiving data frames;

5 a route control module coupled to one of said
6 plurality of fibre channel ports, said route control
7 module for providing an exit port in response to a
8 request from said plurality of fibre channel ports for
9 said exit port, said request comprising a destination
10 identification; and

11 a memory location, said memory location coupled to
12 each of said plurality of fibre channel ports, wherein
13 said memory location stores data frames transmitted to
14 each of said plurality of fibre channel ports, wherein
15 said fibre channel switch has more than one rate for
16 reading and writing data from said memory location to
17 said each of said plurality of fibre channel ports.

1 20. The fibre channel fabric of claim 19, further
2 comprising an interface control module that couples a
3 first fibre channel port and a second fibre channel port
4 of said fibre channel switch, wherein said interface
5 control module provides a first control signal to said
6 second fibre channel switch in response to a second
7 control signal from said first fibre channel switch.

1 21. The fibre channel fabric of claim 19, wherein
2 data frames that are received at a first receiving port
3 of said plurality of ports are written into said memory,
4 and said data frames written into said memory are read
5 from said memory by a first transmitting port of said
6 plurality of ports.

1 22. The fibre channel fabric of claim 19, wherein
2 said memory comprises a plurality of SRAM modules.

1 23. The fibre channel fabric of claim 22, wherein
2 said SRAM modules number 17 in total.

1 24. The fibre channel fabric of claim 19, wherein
2 said memory supports both 1 gigabit per second and 2
3 gigabit per second read and write data rates.

1 25. The fibre channel fabric of claim 24, wherein
2 said memory supports a different read rate and write data
3 rate such that data can be written to said memory at a
4 first rate and simultaneously read from said memory at a
5 second, different rate.

1 26. The fibre channel fabric of claim 19 further
2 comprising a bus coupling said one of said plurality of
3 fibre channel ports to said memory for transmitting said
4 data frame.

1 27. A method for providing a shared memory location
2 coupled to a plurality of ports in a fibre channel switch
3 for buffering and switching data frames from a first port
4 to a second port, said method comprising:

5 providing a plurality of columns of memory, said
6 columns of memory comprising a plurality of rows for
7 storing a portion of said data frames, wherein said
8 portion is written from said first port; and

9 providing a plurality of first-in first out data
10 storage locations, wherein said portion of said data
11 frame is stored in said data storage location before
12 being read to said second port.

1 28. The method of claim 27, wherein the number of
2 columns of memory is equal to or greater than the number
3 of ports.

1 29. A method for providing a shared memory location
2 comprising:

3 receiving data frame at a first port;

4 writing a first portion of said data frame to a
5 first column of memory;

6 reading said first portion of said data and
7 thereafter writing said first portion to a first-in first
8 out storage location; and

9 reading said first portion of said data from said
10 storage location and thereafter writing said first
11 portion to a second port.

1 30. The method of claim 29, wherein said first
2 portion of said frame comprises a word.

1 31. The method of claim 30, wherein said word is 34
2 bits in length.

1 32. The method of claim 30, wherein said writing to
2 the first column of memory is at a first data rate and
3 the reading from the first column is at a second data
4 rate, wherein said first data rate is different than said
5 second data rate.

1 33. The method of claim 32, wherein said first data
2 rate is two gigibits per second and said second data rate
3 is one gigibit per second.

1 34. The method of claim 32, wherein said first data
2 rate is one gigibit per second and said second data rate
3 is two gigibits per second.

1 35. A shared memory location within a fibre channel
2 fabric having a plurality of ports, said shared memory
3 coupled to said plurality of ports, said shared memory
4 comprising:

5 a plurality of memory locations, each memory
6 location comprising a column and having a plurality of
7 rows for storing a data frame, said data frame comprising
8 a plurality of words; and

9 a plurality of first-in first out data storage
10 locations, wherein a word is written from said memory
11 location to said first-in first-out storage location
12 before transmission to a port.

1 36. The shared memory location of claim 35, wherein
2 the number of memory locations is greater than or equal
3 to the number of ports.

1 37. The shared memory location of claim 35, wherein
2 the number of memory locations is an odd number.

1 38. The shared memory location of claim 35, wherein
2 the memory locations are implemented using SRAM modules.

1 39. The shared memory location of claim 35, wherein
2 the width of said memory location is 34 bits, wherein 34
3 bits is the length of said word of said data frame.

1 40. The shared memory location of claim 35, wherein
2 said plurality of said first-in first-out storage
3 locations comprises two first-in first-out storage
4 locations.

1 41. The shared memory location of claim 35, wherein
2 the depth of a buffer is determined by multiplying the
3 number of frames per port by the number of ports by the
4 number of rows per frame.

1 42. The shared memory location of claim 35, wherein
2 the number of rows per frame is determined by dividing
3 the frame byte size by the total resulting from
4 multiplying the number of columns by the number of bytes
5 per word.